Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet	1	of	1

Complete if Known	
Application Number	10/606511
Filing Date	June 25, 2003
First Named Inventor	Jeffrey P. Rupley
Art Unit	2181
Examiner Name	TREAT, William M.
Attorney Docket Number	42P15757

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
WMT		"PowerPC 603 Risc Microprocessor Technical Summary", Freescale Semiconductor, 1994, available at http://www.freescale.com/files/32bit/doc/data_sheet/MPC603.pdf	

Examiner Signature	W. TREAT	Date Considered	4/30/2006

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

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WMT		"Heads and Tails: A Variable-Length Instruction Format Supporting Parallel Fetch and Decode", Heidi Pan and Krste Asanovic, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001), Atlanta, GA, November 2001.	
WMT		"High-Performance Variable-Length Instruction Encodings", Heidi Pan, M.Eng. Thesis, Massachusetts Institute of Technology, June 2002.	
WMT		"Instruction Fetch Mechanisms for VLIW Architectures with Compressed Encodings," Thomas M. Conte, et al., Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture, Paris, France, pages: 201 – 211, 1996	

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Based on PTO/SB/08B (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 08/11/2003.
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